A Radiation-hard Phase-Locked Loop

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***Abstract* — Phase-Locked Loops (PLLs) are often used as frequency multiplier for generating high frequency clock signals. In space application, however, performance of the normal PLL will be degraded due to the radiation effects. In this paper, several aspects of a rad-hard PLL are investigated, including radiation effects, radiation hardening techniques, PLL building blocks and the overall performance.**

This circuit is developed using the Peregrine 0.50um SOS/SOI process. The post-layout simulation result indicts that the circuit can be used to generate 100M-180MHz programmable clock signal under radiation conditions with process, temperature and voltage variations. The maximum peak to peak jitter is less than 100 ps while the maximum lock-in time is less than 20 us under typical conditions.

***Index Terms*— PLL, radiation.**

I. INTRODUCTION

Phase-Locked Loops(PLLs) are used widely as frequency multipliers for generating high frequency. Many digital signal processors (DSPs) and high performance micro-controllers apply PLLs as its internal clock generation circuits. The on-chip Phase-Locked Loops can be easily controlled to have different frequency outputs which are suitable from both performance and power comsumption points of view.

At the same time, space applications such as deep space satellites require the circuits to have high stabilities in the radiation environment. As shown in previous research [2], [3], and [4], semiconductor devices exhibit undesirable characteristics when exposed to radiation. These variations include threshold voltage shifts, single event effects, larger leakage current, and mobility degradation. In order to achieve high stability, special techniques are needed to "harden" the circuit against radiation. These techniques include special process, circuit design techniques and layout considerations. Such circuits are referred as "rad-hard" circuits.

In this paper, a programmable rad-hard PLL circuit was designed to generate high frequency clock signals. With special concern for radiation effects, several rad-hard techniques were adopted in this design.

II. RADIATION EFFECT IN VLSI

There is an abundance of photonic and particulate radiation in outer space. Depending on the energy of the particles, they affect semiconductor devices differently. X ray, gamma ray and heavy ion have large amounts of energy that can create a lot of electron-hole pairs in the semiconductor device. On the other hand, the energy of the neutron, proton and electron is too low to generate many electron-hole pairs directly, however they can cause silicon atoms to recoil and act as heavy ions. [2], [3] These effects will cause some big impacts on semiconductor devices as follows.

A. Threshold Voltage Variation due to holes trapped in SiO2

When an ionizing particle strikes a MOS transistor, electron-hole pairs are generated. The electron-hole pairs quickly disappear in the gate (poly-silicon or metal) and in the substrate since these kinds of material have little resistance. However, in the gate oxide, they result in noticeable effects. Some electron-hole pairs will recombine immediately after generated, other electron-hole pairs will move under the electric field formed under the gate. Since the mobility of electrons is much larger than that of holes, the electrons, which don't recombine with holes, will move out of silicon oxide very fast. The holes, however, move very slowly under the electric field to the SiO2-Si interface (if the gate voltage is positive). Some of the holes will even become trapped in the oxide. Because of the extra holes, this oxide will exhibit a positive charge phenomenon. The amount of the trapped charge is directly related to both the density of the radiation and the number of defects in silicon oxide.

The holes trapped in the silicon oxide contribute to the creation of positive oxide charge, $Q_{ox.}$ As the radiation dose increases, the threshold voltage of NMOS devices will decrease and the magnitude of the PMOS threshold voltage will increase. We can model the threshold voltage variation approximately as

$$\Delta V_{thN} = -\frac{Q_{ox} \times (t_{ox} - x_d)}{\varepsilon_{ox}} \quad (1)$$

in which x_d is the distance between Si/SiO2 interface and the charge. If the holes are trapped in the the SiO2-Si interface, threshold voltage variation becomes

$$\Delta V_{thN} = -\frac{Q_{ox} \times t_{ox}}{\varepsilon_{ox}} \quad (2)$$

Thus, the change of threshold voltage is proportional to the dose rate (density) of radiation and the square of the thickness (t_{OX} of the gate oxide).

B. Threshold Voltage Variation due to Si/SiO2 surface change

Another effect of radiation on MOS transistors is the radiation-induced traps at the interface of Si/SiO2 [4]. This phenomenon has been studied extensively, but is still not

fully understood. Unlike the traps in the silicon oxide, which are always positive, the traps at the interface of Si/SiO2 present negative charges for NMOS and positive charges for PMOS.

The charges trapped in the Si/SiO2 interface can be ignored under low radiation density since it is much less than the charges trapped in the silicon oxide and has little effect. However, in high radiation cases, the traps in the Si/SiO2 interface cannot be ignored. They will operate differently than the holes trapped in the oxide. For the NMOS device, since these traps are donor-like, they will increase the threshold voltage. However, for PMOS devices, since these traps are acceptor-like, they will increase the absolute value of the threshold voltage.

At the same time, the number of holes trapped in the oxide is related to the recombination ratio of the hole-electron pairs. The mobility of the holes determines the recombination ratio, with the higher the mobility of the holes, the fewer hole-electron pairs recombine (The typical mobility of an electron in silicon oxide at room temperature is 20 $cm^2\ V^{-1}s^{-1}$ while the mobility of a hole in silicon oxide is much lower, varies from 10^{-4} to 10^{-11} $cm^2\ V^{-1}s^{-1}$ [4]). Because the mobility of the hole is strongly dependent on temperature and electric field strength, the change of threshold voltage is also related to gate voltage and temperature.

C. Single Event Effects (SEE)

Single event effects are phenomena caused by the penetration of a highly energetic particle, such as a heavy ion, to the semiconductor device. These phenomena may completely destroy the logic state of the related transistor, thus affecting the proper operation of the whole system.

The most common Single Event Effect is the single event upset (SEU) [5]. When an energetic ion strikes a MOS transistor, it may distort the depletion region near its track. Since a lot of electron-hole pairs are generated along the track, some electrons in the distorted depletion region will drift to the junction while the holes will move towards substrate. These electrons create drift current which lasts a very short time (order of 0.1ns). Another current will also be generated after the drift current. That current is caused by the diffusion of the electrons under the depletion area. As shown in the Fig. 1, these electrons will diffuse slowly toward the depletion area after the penetration of the energetic ion. This current is called diffusion current or "delay current". The magnitude of the diffusion current is much smaller than the magnitude of the drift current, but it last longer (on the order of a hundred ns) than that of the drift current [6]. These two currents may upset the current logic state of the related node and cause the entire circuit to malfunction.

In SOI process, however, SEE has less impact in SOI MOSFETs. If an energetic ion strikes the SOI MOSFET, a large amount of electron-hole pairs will be generated similarly to the CMOS devices as discussed above. However, most of the electron-hole pairs generated in SOI devices will end up in the substrate, which is isolated from the transistors by the buried oxide, thus reducing the chances of upsetting the logic state of the affected node.

D. Other Radiation Effects

Besides threshold voltage variation and the singe event effects, radiation effects also include the larger subthreshold current, the larger leakage current, and the degraded mobility.

Different circuits may have different performance degradation under radiation. Normally, digital circuits are more sensitive to the single event effect, which may upset the logic state. On the other hand, the performance of the analog circuit may easily be affected by the threshold voltage variation.

III. A PROGRAMMABLE RAD-HARD PLL

Fig. 1 shows a typical PLL circuit diagram for frequency multiplication application. It mainly includes four parts: phase detector, loop filter (LF), voltage controlled oscillator (VCO), and divider stage [7], [8]. Because of the negative feedback structure, the PLL will finally achieve a stable state ("locked" state). Once the locked state has been achieved, the output clock is N times faster than the reference clock as shown in the Fig. 2.

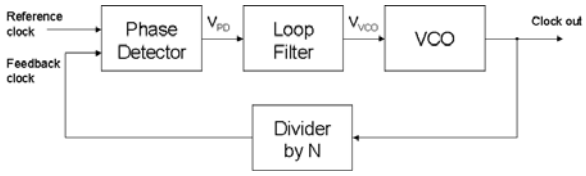

Fig. 1. Block diagram of a typical PLL circuit.

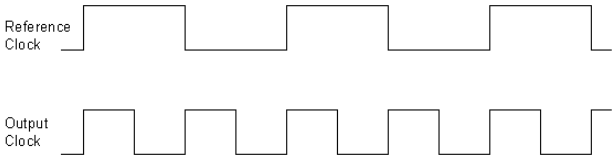

Fig. 2. PLL in locked state (N=2).

Fig.3 shows the circuit diagram of the programmable rad-hard PLL. The PLL includes a phase frequency detector, a charge pump, a loop filter, a voltage controlled oscillator, a divide-by-two stage and a programmable divider.

The Phase Frequency Detector (PFD) compares the difference between the rising edge of the reference clock and the rising edge of the feedback clock. The Charge Pump (CP) converts the pulse signal generated by the PFD to a current signal. The Loop Filter (LF) generates a voltage signal from the input current pulse. The Voltage Controlled Oscillator

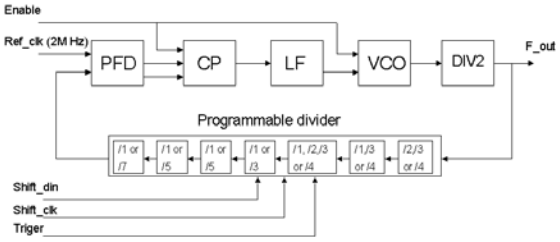

Fig. 3. Circuit diagram of a programmable rad-hard PLL.

converts the input control voltage to a frequency signal. The Div2 block divides the VCO output frequency by 2. It is used to obtain an exact 50% duty cycle. The programmable divider controls the dividing ratio in the feedback loop. The output frequency is determined by the divide ratio.

The PLL circuit consists of both analog and digital circuit. As shown in Fig.3, the charge pump, loop filter, and the VCO are mainly analog circuits. They are sensitive to the threshold voltage variation. But because of the feedback nature of the DLL, it will have stable output if the output frequency doesn't exceed the operation range. The PFD is a digital circuit. It is sensitive to the Single Event Effect (SEE). But the failure will not cause big frequency distortion at the output node and correct operation will be recovered soon. The programmable divider, on the other hand, is easily affected by the radiation effect. If the logic state changed in one of the node because of the SEE, the error may be accumulated and causes the malfunction of the whole system.

A. Basic Logic Gate and its Hardening

The basic inverter circuit is shown in Fig. 4(a). After irradiation, the transfer curve of the basic inverter changes as shown in Fig. 4(b). The most notable changes include the variation of the switch point, the decreased output rail voltage, and the increased leakage current. The proper logic operation may fail if radiation becomes strong enough.

These changes are mainly caused by the variation of the threshold voltage. After irradiation, the threshold voltage of a NMOS transistor typically decreases and the threshold voltage of PMOS transistors typically increases. The decreased threshold voltage of NMOS transistors makes the NMOS very difficult to cut off, even as the gate voltage approaches VSS.

Several solutions have been proposed in [2]. The main idea to recover the output voltage is to make Vgs negative when the NMOS cuts off. Such an example is shown on Fig.5. The additional PMOS and NMOS transistors keep the original NMOS cut off when the input is low and maintain the proper operation when the input is high.

B. Phase Frequency Detector

An improved PFD circuit is shown in Fig. 6(a) [9]. It consists of two modified D-latches and a NOR gate. Each D latch can be implemented using 18 transistors.

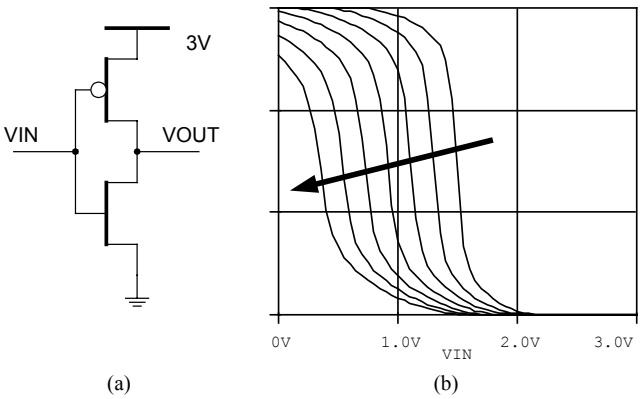

Fig. 4. Inverter Circuit (a) and input vs. output curve (b).

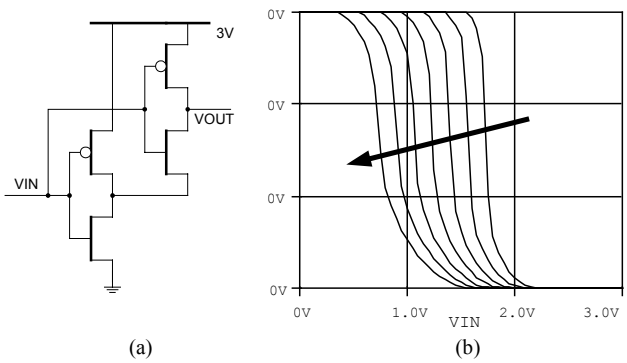

Fig. 5. The modified inverter circuit (a) and curve (b).

The input and output timing of the PFD is shown in Fig. 6(b). When both inputs ref_clk and feedback_clk are rising at the same time, NQ1 and NQ2 will become low after several gate delays. Because the reset signal is low at that time, both the UP and Down output will change to high after one NOR gate delay. Since the reset signal will change to high after one NOR gate delay when the NQ1 and NQ2 are low, UP and Down output will stay high for only one 2-input NOR gate delay. Thus, it minimizes the pulse width when there is no input phase difference and further reduces the jitter

In order to achieve radiation hardening, all gates are redesigned similar to the rad-hard inverter mentioned above. The rad-hard NAND gate and AND-NOR gate are shown in Fig. 7. Additional PMOS and NMOS pair is added for each NMOS.

C. Charge Pump

Charge Pumps are used to convert the pulse signals from the PFD to a current signal. That current is used to generate voltage signal for controlling the VCO through the loop filter.

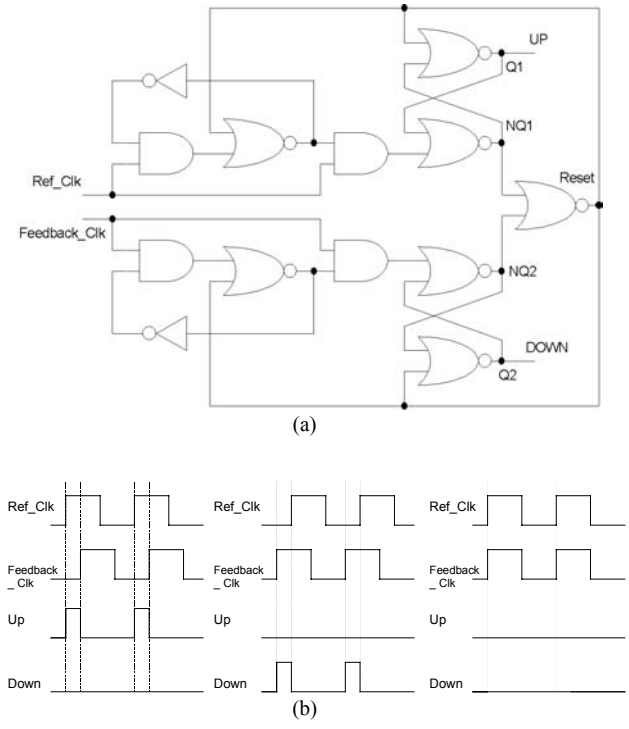

Fig.6. The improved PFD circuit (a) and timing (b).

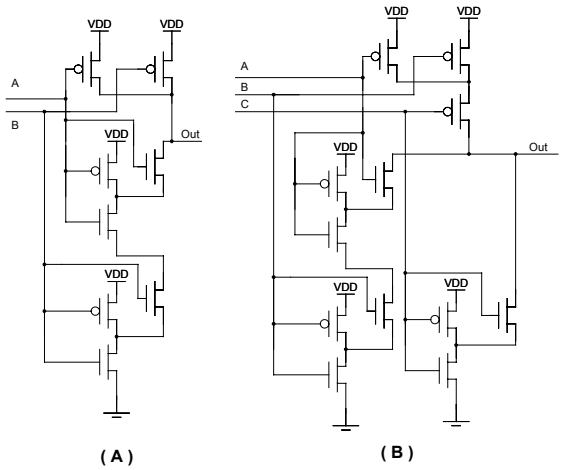

Fig. 7. The rad-hard NAND gate (a) and AND-NOR gate (b).

Fig. 8 shows the detailed circuit schematic of a charge pump [10]. In this circuit, M5 – M8, D1, D2 and R1 are used to provide a stable current source. It uses the thermal voltage referenced self-biasing technique. The output current is

$$I = \frac{nV_T \times \ln K}{R_1} \tag{3}$$

where n is a constant value, in the range from 1.0 – 2.0 depending on process, V_T is the thermal voltage and equal to 25.6 mV, and D2 has an emitter area K times larger than D1.

Since the value of current source is not dependent on the threshold voltage, it is relatively stable in a radiation environment when all the MOSFET drift in the same way.

M1-M3 are used to trigger the current source to operate when the power is turned on and the charge pump is enabled. The charge pump circuit can operate under both large and small current. It is realized by switching transistors M13 and M14. When these two transistors are turned on, the current flow through M23 or M24 is about 160uA when the UP or Down signal is enabled. When M13 and M14 are turned off, the output current is only 40 uA. The large and small current is controlled by the input control signal, HCURRENT. The large current is generally used when the PLL begins operation. It can significantly reduce the lock in time. The small current is used when the output becomes stable. Thus the phase difference will only make fine adjustments in the control voltage and further reduce jitter in the output.

The output stage includes transistors M17 – M25. It mirrors the current from the current source. The UP and Down inputs are used to control the output to source or to sink current through the current source.

The whole charge pump circuit can be disabled through input labeled Enableb. This function can be used in the power save mode when the high frequency output is not needed.

D. Loop Filter

The loop filter used in this circuit is a typical loop filter circuit for PLL as shown in Fig.9, which works as a low pass filter. If there are small variations in the input current, the current I_{PD} linearly charges C1 and C2. This results in an averaging effect. For fast variations, since C1 is much larger than C2, the current I_{Pd} appears as though it simply drives the resistor R, eliminating the averaging effect. Thus allowing the PLL to track quickly for the large phase differences. The values of the capacitors and resistor determine the PLL's overall dynamic response.

The lock range ($\Delta\omega_L$), which is the range of the frequencies in which the PLL for normal operation, equals to

$$\Delta\omega_L = 4\pi\xi\omega_n \tag{4}$$

Where ξ is the dumping factor and ω_n is the natural frequency.

$$\xi = RC_1\omega_n / 2 \tag{5}$$

$$\omega_n = \sqrt{\frac{K_{PFD}K_{VCO}}{NRC_1}} \tag{6}$$

Where KPFD is the gain of the PFD, KVCO is the gain of VCO. N is the frequency divider ratio in the feedback loop.

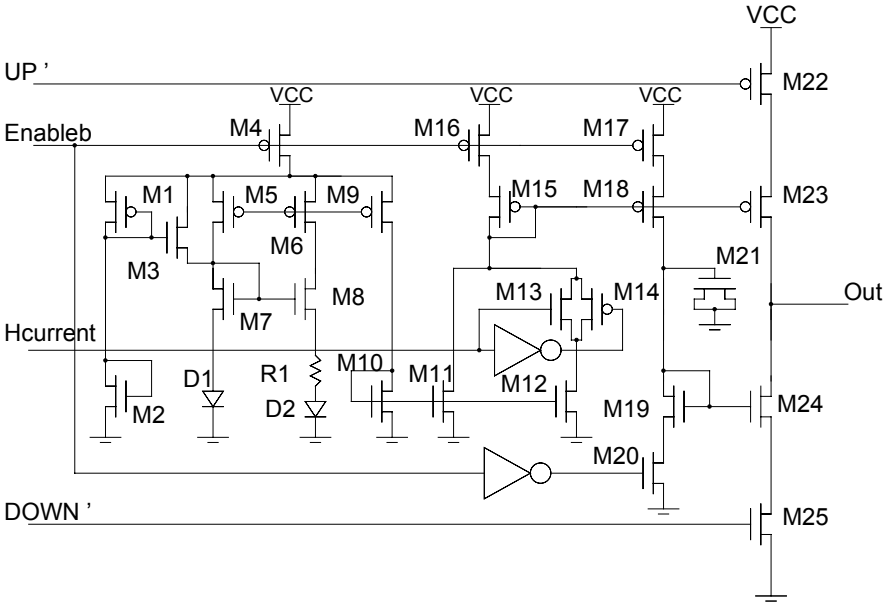

Fig. 8. A charge pump circuit.

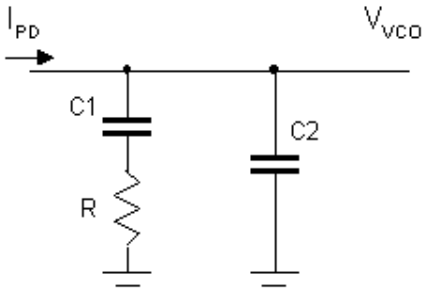

Fig. 9. Loop filter used in the PLL circuit.

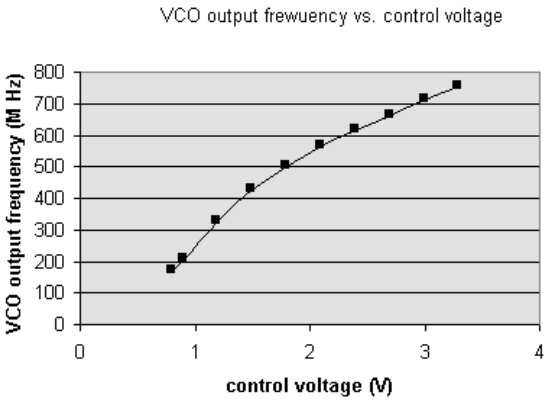

Fig. 11. VCO characteristics.

E. Voltage-Controlled Oscillator

The voltage-controlled oscillator (VCO) is the key part of PLL. It converts the voltage control signal to a proportionate frequency. The VCO circuit is designed to cover the frequency range from 200 MHz– 350 MHz over process variation, temperature variation, supply voltage variation, and the radiation effects.

The VCO circuit is shown in Fig.10. It includes two current-controlled ring oscillators (M12-M23, M24-M35) for noise rejection purpose [10]. Each ring oscillator includes three inverters, and each inverter consists of four transistors for rad-hard purposes. The total current of oscillators is provided by M3 and M5-M8. Transistor M3 converts the control voltage to current while M5-M8 provide minimum current for ring oscillators when M3 is off. The sum of the current is mirrored through M10, M11 and then controls the ring oscillators.

The cross-coupled transistors M28, M29 synchronize the two oscillators so that the outputs are 180-degrees out of phase. The simple diff-amp (M38-M42) converts the outputs of two ring oscillators to a single ended value and restores the VCO output voltage swing to full rail-to-rail output [10].

The VCO characteristic in typical condition is shown in Fig. 11. The range of output frequency is larger than the required range. The maximum output frequency is far beyond the requirement to provide enough margins for temperature variation, power supply variation and radiation effects.

F. Programmable Counter

The programmable counter consists of seven dividers as shown in Fig. 12. The divide ratio of every divider can be selected from several values. Certain combination value is chosen to achieve both high resolution and small size. A 10-bit input word is used to control these divide ratios. That data is input through a shift register using inputs Shift_din and Shift_clk. Input trigger informs the PLL to accept the new input data to control the programmable counter. The new input data will become valid at the rising edge of the trigger signal.

The programmable divider is easily affected by SEU because of its large size. An improved circuit shown in Fig.13 reduces effects caused by SEU. Two redundant programmable dividers are used. The final output comes from the vote circuit with inputs from three programmable dividers. The three clock signals for programmable dividers have the same frequency but at different phases to provide additional hardening resistance [11]. These three phase clock signals come from the output of VCO using the circuit shown in Fig. 14.

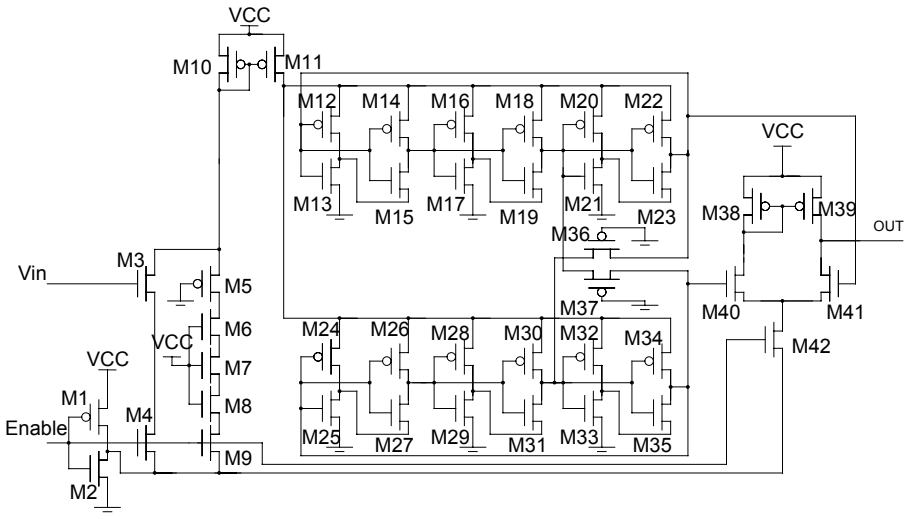

Fig. 10. The VCO circuit.

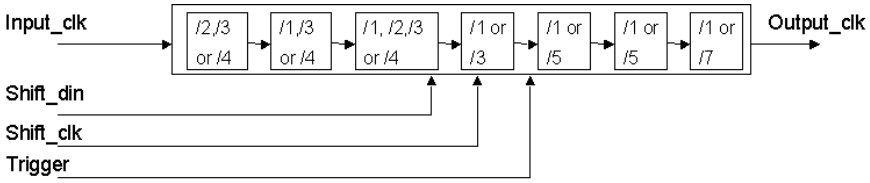

Fig. 12. Programmable counter.

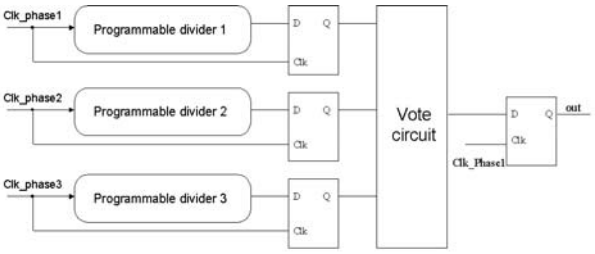

Fig. 13. Rad-hard programmable divider circuit.

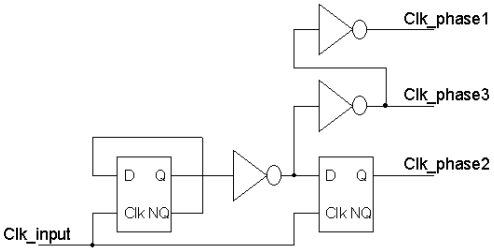

Fig. 14. Three phase clock signals generating circuit.

IV. SIMULATION RESULT

Two major radiation effects can be evaluated through simulation. One is the threshold voltage variation and the other is the mobility degradation. For BSIM 3V3 model, threshold voltage variation can be simulated by adjusting Vth0 while the mobility degradation can be estimated by adjusting U0. In simulations for radiation effect, Vth0 adjusts –20% for NMOS and +20% for PMOS (absolute value). U0 adjusts –10% for both transistors. These variations are similar to the radiation effects when total dose volume is about 100 K – 1M Rad [12].

The summary of the final simulation result is shown in Table I. The output frequency range covers 100M – 200MHz in most situations.

TABLE I
SIMULATION RESULTS.

output frequency range (pre-layout)	100 M - 350 MHz (Typical at 27 °C, 3.3 V, without radiation)
	100 M – 220 MHz (with process, power supply and temperature variation; include radiation effect)
output frequency range(post-layout)	80 M – 280 MHz (Typical at 27 °C, 3.3 V, without radiation)
	100 M – 180 MHz (with process, power supply and temperature variation; include radiation effect)
Power Consumption	1.8 mA (divide ratio = 64, typical), 2 nA (Power save mode)
Maximum jitter	< 100 ps (divide ratio = 64, typical)
Lock in time	< 20 us (divide ratio= 64, typical, jitter< 100 ps)

V. CONCLUSION

A Phase-locked loop (PLL) circuit is designed using rad-hard techniques. The simulation results indicate that the circuit can be used to generate 100M-180MHz programmable clock signal under radiation conditions with process, temperature (0-70°C) and voltage (3.0V-3.6V) variations. The maximum peak-to-peak jitter is less than 100ps while the maximum lock-in time is less than 20 us under typical conditions.

VI. ACKNOWLEDGMENT

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